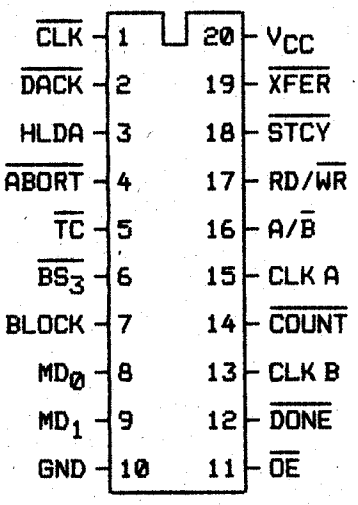
- **Coupled with 16R801 IEEE-696 Bus State Sequencer and 16L801A IEEE-696 DMA Priority Comparator generates all cycle timing for high performance IEEE-696 DMA controller**
- **Generates timing signals for block transfers, block initialize, and block search functions**
- **Byte by byte or continuous DMA transfer modes**

16R802, 16R802A
TOP VIEW



description

The 16R802 coupled with the 16R801 IEEE-696 Bus State Sequencer and the 16L801A IEEE-696 DMA Priority Comparator form the heart of a high performance DMA controller for the IEEE-696 bus. With external address counters, a byte transfer counter, an 8-bit data latch and a few gates, the two-port DMA controller is complete. With this configuration, block memory (or I/O) transfers and block initialization is possible. Block searches are possible with the addition of a comparator.

pin description

CLK **Clock input.** All timing is referenced to the falling edge of this clock.

DACK **DMA Acknowledge input.** (from 16L801A) Active low. If low and HLDA is high, causes the 16R802 to execute a command on the next falling edge of CLK.

HLDA **Hold Acknowledge input.** Active high. Same as the IEEE-696 HLDA signal.

ABORT **Abort command input.** Active low. Causes termination of the current command and supresses clocking of address counters and the byte transfer counter. This input is normally used by a comparator circuit in the block search mode.

$\overline{TC}$ **Terminal count input.** Active low. Causes termination of the current command. Address counters and the byte transfer counter are clocked in the normal manner. This input is connected to the terminal count output of the byte transfer counter.

$\overline{BS_3}$ **Bus state three input.** (from 16R8Ø1) Active low. Used to signal the DMA controller that the current bus cycle will terminate on the next clock. During BS_3, $\overline{ABORT}$ and $\overline{TC}$ are sampled to decide whether or not to start a new bus cycle.

MD_1, $MD_Ø$ **Mode select inputs.** Selects one of four operation modes according to the following table:

MD_1	$MD_Ø$	SYMBOLIC	MODE DESCRIPTION
Ø	Ø	(A)	Read A
Ø	1	–> (A)	Write A
1	Ø	(A) (B)	Read A, read B
1	1	(A) –> (B)	Read A, write B

$\overline{DONE}$ **Command done output.** Active low. Goes low for one clock after the current DMA operation is completed. If BLOCK is high, $\overline{DONE}$ goes low when the entire transfer is done.

$\overline{COUNT}$ **Count down byte transfer output.** Active low. Goes active for one clock to decrement the byte transfer counter. Either the rising or falling edge of this signal can be used to clock the byte transfer counter.

CLK A / CLK B **Address counter A / Address counter B clock outputs.** The rising edge of CLK A or CLK B should increment (decrement) the appropriate address counter.

A/$\overline{B}$ **Port A / port B select output.** Selects address counter A if high or address counter B if low. Qualified with $\overline{BC}$ from the 16R8Ø1, A/$\overline{B}$ should enable the appropriate address counter onto the address bus.

RD/$\overline{WR}$ **Read / write control output.** Active high. This signal is high if the next bus cycle is a read cycle, and a write cycle if low. This signal is connected to the RD/$\overline{WR}$ input to the 16R8Ø1.

$\overline{\text{STCY}}$ **Start bus cycle output.** Active low. This signal connects to the $\overline{\text{STCY}}$ input of the 16R801, and is used to initiate bus cycles.

$\overline{\text{XFER}}$ **Transfer state active output.** Active low. Active when the bus control signals are to be gated onto the control bus. This also applies to the XS I and XS II states of the IEEE-696 DMA protocol where both the permanent master and the temporary master drive the control bus.

recommended operating conditions

PARAMETER	16R802 16R802A			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
Low-level output current, I_{OL}			24	mA
High-level output current, I_{OH}			-3.2	mA
Operating free-air temperature	0		70	deg C

electrical characteristics over operating conditions

PARAMETER		TEST CONDITIONS		16R802 16R802A			UNIT
				MIN	TYP	MAX	
V_{IL}	Low-level input voltage					0.8	V
V_{IH}	High-level input voltage			2.0			V
V_{IK}	Input clamp voltage	V_{CC} = MIN I_I = -18mA			-0.9	-1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.4V			-20	-250	uA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V				25	uA
I_I	Maximum input current	V_{CC} = MAX V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX I_{OL} = MAX V_{IH} = MIN				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN		2.4	3.5		V
I_{OZ}	Off-state output current	V_{CC} = MIN V_{IL} = MAX I_{OH} = MAX V_{IH} = MIN	V_O = 0.4V V_O = 2.4V			-100 100	uA
I_{OS}	Short-circuit output current	V_{CC} = 5V		-30	-60	-90	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

switching characteristics over operating conditions

TEST CONDITIONS: R_1 = 200 ohms, R_2 = 390 ohms, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	16R802A			16R802			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns
t_{PLH} t_{PHL}									ns